Integrated Circuits and Intellectual Property Rights in India

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The Semiconductor Integrated Circuit Layout-Design Act, 2000, protects original, inherently distinctive layout-designs that have not been previously commercially exploited and registration is a necessary pre-requisite for protection. A layout-design is original if it is not merely a copy of all, or substantial part of another layout-design, and is the result of the creator’s own intellectual effort. Registration of a layout-design shall be available to the registered proprietor irrespective of the fact whether the layout-design is incorporated in an article or not. The Act makes provision for a registry to be headed by a Registrar for the purpose of registration of layout-designs. Protection under the Act extends for ten years and commences from the date of application for registration in case of layout-designs which have not been commercially exploited. For layout-designs, which have been commercially exploited (for less than two years) before the date of application for registration, protection commences retrospectively from date of first commercial exploitation. The registered-proprietor has the exclusive right to reproduce by any means the registered layout-design or any substantial portion of it. But the Act permits ‘reverse-engineering’ of a layout-design for limited purposes. The registered-proprietor also has the exclusive right to import, sell or distribute for commercial purpose any semiconductor chip products in which the registered layout-design is embodied. The Act provides for criminal remedies for the infringement of a layout-design expressly, civil remedies too are available to enforce rights under the Act. A registered layout-design can be assigned or transmitted with or without the goodwill of the business concerned. Registration of assignment or transmission is necessary to establish title to the registered layout-design. The Act also provides for reciprocal arrangements between convention countries. This article endeavours to examine the nature of the intellectual property involved in layout-designs, their use in semiconductor integrated circuits and the other relevant provisions of the Act.

Keywords: Integrated circuits, layout designs, semiconductors, TRIPS

The Semiconductor Integrated Circuits Layout-Design Act, 2000 (the ‘Act’) gives recognition to a new form of intellectual property, namely, the 'layout-designs' used in semiconductor integrated circuits as has been defined u/s 2(h) of the Act.

Exchange of information on a worldwide basis now can occur instantaneously because it can be stored so readily and in such quantities in semiconductor integrated circuits or chips as they are commonly known, has far reaching implications for privacy, international relations, national security and defense. Chips are often referred to as ‘the crude oil of the information age’.2

The simplest integrated circuit consists of three layers, one of which is made from semiconductor material. A wafer (i.e. a thin, highly polished silicon crystal disk) of semiconductor material is coated with a layer of silicon oxide (an insulator) and the electronic components (for example, transistors) are formed by a process of diffusion (chemically doping the semiconductor material with impurities through holes etched through the oxide). Finally, an aluminium coating is applied which is partly evaporated using a mask, leaving behind the interconnections between components formed in the semiconductor layer. It might thus be said that that the information highway is paved with silicon.

The mask is transparent except for opaque patterns on the mask that correspond to the circuit patterns to be etched into the wafer. In a complex circuit, another layer of silicon is placed on top of the etched wafer, and the same etching process is repeated. A chip typically has eight to twelve layers, each layer having a unique mask creating the required circuits. These layers of masks, collectively called ‘mask work’ or ‘layout-design’, manifest the three-dimensional layout of the chip. It is a chip’s layout, or three-dimensional organization that requires protection. In more advanced manufacturing systems, the actual physical mask may be dispensed with and the semiconductor material may be subjected to a controlled light beam which effectively traces out (in raster fashion) a mask.

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for each layer of the chip. Hereafter, references to ‘masks’ should be read as including the stored information used in controlled light beam, as well as the more conventional photographic type physical ‘mask’.

**Chip Piracy and Need for Protection**

The layout-designs of integrated circuits are creations of human mind. It takes enormous investment, both in terms of time and money, to design a new layout-design. But a chip pirate can easily replicate the layout-design of a chip in few months by removing the chips plastic/ceramic casing and photographing each layer of the translucent silicon material; at a fraction of the original cost.

Before 2003, the legal framework relating to copyright, patent or industrial designs did not afford adequate protection to layout-designs. Firstly, protection of layout-designs demands more stringent norms of originality than those required under the Copyright Act. The Copyright Act is too general to accommodate the original ideas of scientific creation of layout-designs. Also whilst it may well have been the case that any design drawings and the masks used in the production process would benefit from copyright protection, the status of the finished product was less clear. Just as copyright in an architectural plan does not prevent anyone from building the house represented in that plan, copyright in the technical drawings representing a chip design does not protect against unauthorized duplication of the chip itself. Secondly, for an article to receive a patent, its design must be novel and non-obvious. This high standard of inventiveness required of patentable articles is rarely achieved in what is essentially the spatial organization of commonly known circuit elements. Thus the work involved in chip manufacturing is of a developmental nature rather than an inventive nature and might not qualify for a patent. Thirdly, layout-designs of integrated circuits are not industrial designs because they do not determine the external appearance of integrated circuits. They determine the physical location, within the integrated circuit, of each element having an electronic function. Thus, the need was felt for sui generis protection.

**Background of the Semiconductor Act, 2000**

Protection to semiconductor chips was first given in the US through Semiconductor Chip Protection Act (SCPA) in 1984 and its impact was felt virtually throughout the world. Japan introduced similar protection in 1985, viz., Japanese Circuit Layout Right Act (JCLRA). An EC Directive, with implementing legislation in all Member States of the EU accelerated international efforts resulting in formulation of 1989 Treaty on Intellectual Property in Respect of Integrated Circuits (IPIC Treaty) under the auspices of WIPO. The IPIC Treaty was later made part of the TRIPS Agreement. TRIPS called for adherence to most of the substantive provisions of the IPIC Treaty. As member of TRIPS Agreement, India has enacted the Semiconductor Integrated Circuit Layout-Design Act, 2000, but it has yet to come into force. The implementation of the Act comes under the Ministry of Communication and Information Technology. A layout-design has to be registered to receive protection under the Act.

**Subject Matter of Protection**

The Act affords protection to the layout-design of a semiconductor integrated circuit. Protection is given to the layout-design itself, so that design houses producing layout-designs would have protection for those products separate from their incorporation in a chip product. On the contrary in USA, a mask work is not eligible for protection unless and until it is fixed in a semiconductor chip product. A mask work is ‘fixed’ according to section 901(a)(3) of the SCPA, in a semiconductor chip product “when its embodiment in the product is sufficiently permanent or stable to permit the mask work to be perceived or reproduced from the product for a period more than transitory duration.” Thus, a mask work will ordinarily be fixed in a semiconductor chip product once the first product has been manufactured.

But under Article 2(ii) of the IPIC Treaty, ‘layout-design’ has been defined as “the three-dimensional disposition, however expressed, of the elements, at least one of which is an active element, and of some or all of the interconnections of an integrated circuit, or such a three-dimensional disposition prepared for an integrated circuit intended for manufacture.” Thus, from this too, it becomes clear that there exists no need for the design to have been implemented in physical form as the words “or such a three-dimensional disposition prepared for an integrated circuit intended for manufacture” have been included in the definition. The same intention can be imputed to the Indian Legislature while it was drafting the Act. The explanation to Section 17 also lays down that the right conferred by the registration of a layout-design shall be available to the registered proprietor.
irrespective of the fact whether the layout-design is incorporated in an article or not. Moreover, India is a member of the TRIPS Agreement which itself obliges adherence to Article 2 through 7 [except Article 6(3)] of the IPIC Treaty. This proposition gathers force from the fact that there are specialist design houses which prepare the layout-design of an application-specific integrated circuit (ASIC) for a customer, the topography being implemented in a separate semiconductor foundry. Clearly, it is important for the layout-design to be protected at this stage, and not merely after its implementation in a semiconductor chip product.

Protection under the Act exists only after the layout-design has been registered. Layout-designs can be registered, if they are; (i) original, (ii) inherently distinctive, (iii) capable of being distinguishable from any other registered layout-design and (iv) if they have not been commercially exploited for more than two years before date of application for registration.

Thus, the Act does not require ‘novelty’ (as in patents) but ‘distinctiveness’ for the purpose of registration.

A layout-design normally consists of a combination of elements and interconnections that are commonly known among creators of layout-designs and manufacturers of semiconductor integrated circuits and hence are considered original only if such combination taken as a whole is the result of its creator's own intellectual efforts. Thus, the Act has recognized that layout-designs will usually contain design elements already existing or protected in the semiconductor industry which is an important issue for semiconductor layout-designs as they are, in the vast majority of cases, new compilations of well-known (i.e., commonplace) elements. The Act calls for ‘creator’s own intellectual effort’ and also lays down that such designs should not be commonplace among the creators of layout designs and manufacturers. This may be shown by the original combination of elements of design that are not by themselves original. Thus, a new topography may be the result of a combination of commonplace elements, which have not been combined in precisely the same way as before. Also, the chances are that any newly designed layout-design which is not simply a copy of an existing design will have at least some features or combination of features which are dissimilar to features already well-known in respect of semiconductor products.

In the case of *Ocular Sciences Ltd v Aspect Vision Care Ltd* attempt was made at understanding what ‘commonplace’ meant. In the Patents Court, Mr Justice Laddie pointed out that the word “commonplace” is not one previously used in UK law (here its meaning as it appeared in the Copyright, Designs and Patents Act 1988 was in question) but derives from the E C Directive on the legal protection of semiconductor topographies. Whilst not wanting to paraphrase a word used in a statute, Laddie J liked counsel’s submission that any design which is ‘trite, trivial, common-or-garden, hackneyed or of the type which would excite no particular attention in those in the relevant art is likely to be commonplace’. However, and in line with the semiconductor Directive, he confirmed that a design, which is made up of a number of such features, need not necessarily itself be commonplace. For protection, the combination must itself not be commonplace and this could be so even if the constituent parts are trivial or mundane.

The need to show ‘intellectual effort’ might be difficult given the use of layout-design, and the fact that the principles of assembling the elements of a layout-design are fairly well established, though the effort involved in doing so might be substantial. Therefore, this originality requirement is stronger than the originality required under the Copyright Act, but weaker than the novelty requirement under the Patents Act. These are drafted along the lines of Article 3(2)(a) and (b) of the IPIC Treaty.

The second requirement is that it must be inherently distinctive or inherently capable of being distinguished from any other registered layout-design. These terms although the same as appearing in the Trade Marks Act, 1999 have different meanings. It must by its very nature be different from other registered designs. Probable tests of inherent distinctiveness could be:

- Function performed by the layout-design is new and different from that performed by other layout-designs. This would make the layout-design distinct in the itself even if it happens to contain some well-known design elements.
- Elements/substances used in the manufacture of the layout-design are novel in the industry, for example, certain new alloys.

This requirement of inherent distinctiveness is found in the Indian Act only, no mention of the same
being found in any previous Act on semiconductor layout-design elsewhere or for that matter in the IPIC Treaty or TRIPS Agreement.

The third requirement is with respect to commercial exploitation. Any act of leasing, selling, offering/exhibiting for sale, a layout-design for any commercial purpose amounts to commercial exploitation. Distributing a layout-design for commercial purposes (and not necessarily for monetary gain) too amounts to commercial exploitation. Thus, the key test is that the activity must be for a commercial purpose. If a scientist was to distribute a tube-light electronic ballast created by him, incorporating a new original layout-design (which enables the tube-light to switch on without blinking, as fast as a bulb, and also function at very low voltages), to fellow colleagues for personal use, it would not amount to commercial exploitation. But if he were to sell it as a new product developed by him, it would amount to commercial exploitation.

**Duration of Protection**

Protection under the Act extends for ten years, which is in line with Article 38(1) of the TRIPS Agreement. While the TRIPS Agreement and the IPIC Treaty are silent on the date of commencement of protection, many of the existing laws on the protection of layout-designs of integrated circuits including, *inter alia*, the laws of USA (SCPA Section 904(a)), of the Member States of the European Union (following Article 7(1) of the Council Directive of December 1986 of the then European Communities; see, for example, Section 5(1) of the German law and Section 8(1) of the Austrian law) provide such protection from the date of the first commercial exploitation, anywhere in the world, where such exploitation has taken place, or, where no such exploitation has taken place, on the date on which the application for the registration of the layout-design was filed or on which it was registered.

Under the Indian Act, it commences from the date of application for registration in case of layout-designs, which have not been commercially exploited. For layout-designs which have been commercially exploited (for less than two years i.e.) before the date of application for registration, protection commences retrospectively from date of first commercial exploitation. But irrespective of when the duration of protection is calculated from, rights can be enforced only after registration. Thus, if a chip was released in the market for commercial exploitation in March 2001 and registered in October 2002, protection would commence from March 2001 for a period of ten years i.e. upto March 2011. Upon registration, the proprietor is, however, entitled to claim damages not only for the infringement of his rights which occurred after October 2002 but also for infringement which occurred from March 2001.

**Exclusive Rights Provided**

The registered-proprietor has the exclusive right to reproduce by any means the registered layout-design or any substantial portion of it. However, there is one significant exception to this exclusive right. Any person may reproduce the layout-design “for the purposes of scientific evaluation, analysis, research or teaching…” This is similar to fair dealing exception in copyright law. The Act also allows persons to ‘reverse-engineer’ layout-designs for the purpose of analysing the layout-designs and incorporating the insights of their analysis into an original layout-design of their own. Such a provision is considered to be justified, in accordance with Article 6(2)(b) of the IPIC Treaty and the provisions in the TRIPS Agreement, as there is a need to encourage creativity through the improvement of existing layout-designs. Moreover, to successfully enter an integrated circuit market segment with a new product, the new entry must usually be compatible with established products. However, the information needed to achieve compatibility is often not publicly available. Thus, aspiring competitors must gather this information another way. However, they must do so without infringing layout-design rights under the Act. In defining acceptable reverse engineering, lawmakers attempted to balance the need for protecting investments in layout-designs with pro-competition sentiment.

The reverse engineering limitations on protection in the US SCPA are found in Section 906(a), (1) and (2); in Article 12(2) of the JCLRA and in regulation 8(4) of the UK Design Right (Semiconductor) Regulations 1989. The US Court of Appeals for the Federal Circuit has held in the case of *Brooktree Corporation v Advanced Micro Devices* that a ‘paper trail does not exclusively prove a reverse engineering defence’ under the SCPA. The Court explained that the statute does not excuse copying where the alleged infringer first tried and failed to reverse engineer a chip layout without copying. The Court rejected the claim that the reverse engineering defence can be established by the sheer volume of paper, pointing
The registered-proprietor also has the exclusive right to import, sell or distribute for commercial purpose any semiconductor chip products in which the registered layout-design is embodied. Thus, the rights under the Act extend not only to the registered layout-design or chips containing such registered layout-designs, but also over products containing such chips, e.g. a watch or cell-phone.

Enforcement of Exclusive Rights

The Act expressly lays down provisions affording criminal remedies for the infringement of a layout-design. But the Act does not provide expressly for civil remedies as in other IP laws nor does it bar these remedies. It merely refers to ‘damages’ in Section 16 which says: “no person shall be entitled to institute any proceeding to prevent, or to recover damages for, the infringement of an unregistered layout-design”. Thus, it can safely be said that the civil remedies, such as injunctions, account of profits and damages would be applicable to enforce rights with respect to layout-designs as well, as in the case of patents, copyright etc. Though it would have been preferable if more express provision to this extent had been incorporated within the Act.

Unlike the law of patents and designs in India (as well as other international instruments for protection of semiconductor topographies), the registered-proprietor has criminal remedies for the infringement of a layout-design. Thus, whoever knowingly or willfully infringes a layout-design shall be punishable with imprisonment upto three years and/or a fine between fifty thousand and ten lakh rupees. In case of infringement, the registered-proprietor is required to submit a written complaint to the Court of Judicial Magistrate First Class, which can take cognizance of this offence. The court may order forfeiture to government of goods related to the offence, and the same may be destroyed in case of a conviction. Again, the Indian Act is distinctive from the existing laws on semiconductor protection. The usefulness of providing for criminal sanctions for intentional acts of infringement lies in the fact that the prevention of infringement of layout-design rights is in the public interest. Criminal sanctions are usually an effective deterrent.

The Act exempts from liability innocent purchasers of infringing chip products with respect to the importation or distribution of those products before they had notice of the layout-design protection. It also allows innocent purchasers who receive notice of infringement, to import or distribute infringing chip products purchased before they had notice, provided they pay the proprietor of the registered layout-design a reasonable royalty.

Assignment, Transmission and Registered Users

A registered layout-design can be assigned or transmitted whether with or without the goodwill of the business concerned. An assignment of a layout-design must be made in writing by the registered-proprietor. No specific form has been prescribed. Transmission means transmission by operation of law, devolution on the personal representative of a deceased person and any other mode of transfer not being an assignment. The law relating to transmission of a layout-design is the same as that for assignment.

In the case of an assignment of a layout-design, without the goodwill of business, the assignment will not take place unless the assignee advertises the assignment in newspapers in accordance with the directions of the Registrar, given on application made for the purpose. Registration of assignment or transmission is necessary to establish title to the registered layout-design.

The Act also provides for the registration of third parties as registered users of the registered layout-design. For this purpose, the registered-proprietor and the proposed user must make a joint application in writing to the Registrar accompanied by an agreement in writing, affidavit made by the proprietor giving details of degree of control by proprietor, place of permitted use, duration of use, etc. Registration as registered user is granted only if the registered-proprietor will exercise proper control over the use of the layout-design by the registered user.

The registered user has a right to use the registered layout-design subject to the conditions and restrictions entered on the register. He may also institute infringement proceedings in certain circumstances. But the right to use is not an assignable or transmissible right. The permitted use by the registered user is deemed to be used by the registered-proprietor. The registered user entry may be cancelled by the Registrar on an application made by the registered-proprietor or the registered user, or any other registered user of the layout-design.

It is important to note that the Act allows the exploitation of a protected layout-design, without the
agreement of the registered-proprietor, by the Government or by third persons authorized by the Government, in public interest (for non-commercial public purposes or for the purposes relating to national emergency or of extreme public urgency) or to remedy an anti-competitive practice. The Government may exploit the protected layout-design without the agreement of the registered-proprietor to whom an adequate remuneration would be paid. For instance, if the nation is engaged in war and requires the use of a specific integrated-circuit to incorporate into its latest long range earth-to-earth missile, but this integrated-circuit consists of a protected layout-design. Then the options available to the Government are to enter into an agreement with the registered-proprietor of such registered layout-design, on commercial terms, for the permitted use of the layout-design, or to approach the Appellate Board to permit compulsory usage.

Conclusion

The enactment of this Act fulfills India’s obligations under the TRIPS Agreement as the Act fulfills the TRIPS norms. This Government initiative to protect integrated circuits will build confidence in the industry and global investing community. The Act compares well with overseas enactments in all important aspects, at times going further even, for example, requirement of inherent distinctiveness and provision of criminal remedies for infringement. The IP regime in India before this Act did not fully cater to the requirements of this specialty area leaving a chip developer with insufficient protection for his work. Recognition of layout-designs for *sui generis* protection will go a long way in benefiting the industry as well as the consumers of chip products by attracting more players in the chip industry and maintaining healthy competition between them, which in turn translates into more competitive pricing. India in itself is slowly emerging as an important player in the multi-billion dollar global semiconductor industry. Indian companies today are claiming to do substantial project work in the area of chip design and have their targets set at making India the design powerhouse of the world. But India being a developing country, considerable foresight and planning are required by the government to institute right policies. TRIPS obliges a high level of IP protection, which should ensure a secure legal environment to encourage such innovative activity.

References

1. This Act was primarily enacted to comply with TRIPS and yet remains to come into force
2. A J W Van de Gevel, From confrontation to competition in the globalized semiconductor industry, 29 May 2000
3. Development of a new chip can take up to $100 million in front-end costs. It can be pirated at a cost of less than $50,000 – Senate Report No 425, 98th Cong, 2d Session 8 (1984)
4. U/s 59 of The Copyright Act, 1957, though the owner of copyright is entitled to recover damages for infringement, if the construction of such building or structure, has been commenced, plaintiff cannot obtain an injunction to restrain its construction or order its demolition, nor will the building or structure be deemed to be the property of the owner of copyright
5. In the Patents (Amendment) Act, 2005, ‘topography of integrated circuits’ is not an invention under sub-section (o) of Section 3
7. Article 35 of TRIPS obliges adherence to Article 2 through 7 [other than Article 6(3) on compulsory licences], Article 12 and 16(3) of the IPIC
8. Presidential assent has been accorded on the Act on 4th September 2000. For Government notifications and other information, www.mit.gov.in
9. Sec 2(h), ‘layout-design’ means a layout of transistors and other circuitry elements and includes lead wires connecting such elements and expressed in any manner in a semiconductor integrated circuit
10. [1997] RPC 289
11. Software Copyright Law, 4th ed, David Bainbridge
12. In this respect the Act differs from the Patents Act under which even own publication results in a bar to grant of patent
13. Section 17 and 18(1)(a), in accordance with Article 6(1)(i) of the IPIC Treaty
14. Article 18(2), in accordance with Article 6(2) of the IPIC Treaty
15. 977 Federal Reporter, 2d Series 1555 - 1583
16. Section 18(1)(b), in accordance with Article 6(1)(ii) of the IPIC Treaty and Article 36 of the TRIPS Agreement
17. Under the SCPA, an action may be sought in the federal court for infringement. Actual damages and infringer’s profit may be awarded to the mask work owner. Alternatively, the owner may elect statutory damages (upto $250, 000)
18. Section 18(6), Article 37.1 of the TRIPS Agreement